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Impact of BTI Induced Threshold Voltage Shifts in Shoot-through Currents from Crosstalk in SiC MOSFETs

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***Abstract*- In this paper a method for evaluating the implications of threshold voltage (V_{TH}) drift from gate voltage stress in SiC MOSFETs is presented. By exploiting the Miller coupling between two devices in the same phase leg, the technique uses the shoot-through charge from parasitic turn-ON to characterize the impact of Bias Temperature Instability (BTI) induced V_{TH} shift. Traditional methods of BTI characterization rely on the application of a stress voltage without characterizing the implication of the V_{TH} shift on the switching characteristics of the device in a circuit. Unlike conventional methods, this method uses the actual converter environment to investigate the implications of V_{TH} shift and should therefore be of more interest to applications engineers as opposed to device physicists. Furthermore, a common problem is the underestimation of the V_{TH} shift since recovery from charge de-trapping can mask the true extent of the problem. The impact of temperature, the recovery time after stress removal and polarity of the stress has been studied for a set of commercially available SiC MOSFETs.**

I. Introduction

Bias Temperature Instability (BTI) is a well-known problem in insulated gate power devices. It is a more critical problem in SiC due to the reduced band offsets between the gate oxide and the wide bandgap semiconductor [1-3], as well as the increased interface trap density [4-6] resulting from the presence of carbon during the oxidation. Positive charge trapping from negative gate bias stress causes a downward shift in the threshold voltage (V_{TH}) referred to as Negative Bias Temperature Instability (NBTI). Negative charge trapping from positive gate bias causes an upward shift in the threshold voltage referred to as Positive Bias Temperature Instability (PBTI). The result of a positive shift in threshold voltage is slightly increased conduction losses. The potential negative consequence from a downward shift in threshold voltage is a converter phase short circuit. In applications that use negative standby/OFF-state voltages to suppress false-triggering, threshold voltage drift under negative gate voltages is a major reliability concern [7]. What is more critical when considering BTI is the potential loss of gate switching synchronization between parallel devices in high current power modules. In high current modules comprised of parallel devices that have undergone unequal V_{TH} shifts due to BTI, the device with the lowest V_{TH} will conduct all the load current assuming the current is being switched from a load that emulates current source over short durations. This can have potentially destructive consequences if the device is taken out of its safe operating area.

There have been various studies on BTI in SiC MOSFETs [8-17]. It has widely been reported that V_{TH} recovery occurs after stress removal [8, 18, 19]. This recovery occurs through the process of charge de-trapping where the captured charge is released over time. It is important to be able to accurately characterize the process of charge capture and release by quantifying the time constants. The time after stress and the threshold voltage recovery after stress is highly relevant to the qualification of power devices. Qualification tests usually require 1000 hours of the device rated gate voltage at 150 °C. Important parameters like V_{TH} and the ON-state resistance must not vary by more than a 20% for the device to be certified as reliable [20]. It is now widely understood that new test methods must be developed for wide bandgap devices since this charge recovery phenomenon can potentially mask the extent of V_{TH} shift i.e. V_{TH} recovery can occur in the duration between the end of the test and the measurement of V_{TH}. To this end, a working committee (JC-70) has been set-up to address this [21]. BTI also has implications in the use of Temperature Sensitive Electrical Parameters (TSEPs) in SiC MOSFETs [22, 23], including the determination of the junction temperature during power cycling [24]. This has led to development of power cycling strategies specific to SiC MOSFETs to overcome this issue [25, 26] with guidelines given in [27]. New characterization techniques for BTI in SiC MOSFETs are required, in order to properly characterize this V_{TH} shift. Different methodologies have been proposed recently as summarized in [28].

In this paper, a more applications-oriented approach is introduced as a means of characterizing BTI in SiC MOSFETs. The method uses a half-bridge power module or 2 discrete devices in a half-bridge configuration. The method is based on "crosstalk" between devices in a phase leg. Crosstalk simply refers to parasitic turn-ON of a power device due to voltage

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commutation of the complementing device in the phase leg [29-32]. The parasitic gate voltage arises due to Miller capacitance feedback that depends on the parasitic gate-drain capacitance C_{GD} capacitance and the gate resistance R_G of the device parasitically switched. This parasitic gate voltage leads to a shoot-through current through the converter phase leg. There has been considerable research effort in evaluating the impact of wide bandgap devices on crosstalk performance [33-35], modelling crosstalk [36, 37] and implementing new methods for minimizing crosstalk [38, 39].

The research presented in this paper uses crosstalk for evaluating the implications of BTI-induced threshold voltage shifts in SiC MOSFETs. By measuring the peak shoot-through current and total shoot-through charge, it is possible to identify V_{TH} shift in SiC MOSFETs that have undergone BTI stress. Section II presents a review on BTI degradation and characterization in SiC MOSFETs, section III describes the experimental set-up used in this paper and presents the characterization of crosstalk for different SiC MOSFETs and section IV demonstrates how the shoot-through current method can be used for detecting BTI-induced threshold voltage shifts in a set of commercially available SiC MOSFETs. Using the proposed method, the transient recovery of V_{TH} after stress removal and the impact of temperature is evaluated in section V while section VI concludes the paper

II. BTI Degradation And Characterization in SiC MOSFETs

Threshold voltage shift caused by gate bias stress in SiC MOSFET has been the subject of different studies in the recent years [1, 2, 8-19, 28, 40-43]. Accelerated stress tests can be performed on SiC MOSFETs to evaluate the reliability and lifetime of the gate oxide [12, 44] and the shift of V_{TH} [45]. The tests are accelerated by using gate-voltages beyond the rating of the device to emulate long stress times at the rated voltage. The stress tests can include both positive and negative high temperature gate bias. The results of the accelerated stress tests for 900 V SiC planar MOSFETs [45] are shown in Fig. 1. Fig. 1(a) shows how the V_{TH} reduces with negative gate bias stress as indicated by a leftward shift in the gate transfer characteristics. Fig. 1(b) shows how V_{TH} increases with positive gate bias stress as indicated by the rightward shift of the gate transfer characteristics. The measurements shown in Fig. 1(a) and Fig.1(b) were obtained from a curve tracer. The static characteristics were measured 16 hours after stress removal to ensure sufficient time for V_{TH} recovery meaning only the permanent shift in V_{TH} was characterized. During the recovery time, V_{GS} was set at 0 V. The gate bias magnitudes, device case temperatures and V_{GS} stress durations are stated in Table I [45].

Accurate measurement of V_{TH} shift while accounting for charge recovery is critical in SiC MOSFETs. In [40] the authors analyze the importance of the measurement speed and delay after stress removal, for both sweep and fast *I-V* V_{TH} measurements. The traditional gate sweep method consists in sweeping the gate-source voltage V_{GS} at a fixed drain-source V_{DS} voltage until the desired drain current I_D is obtained, whereas the fast *I-V* V_{TH} measurement consists in measuring I_D

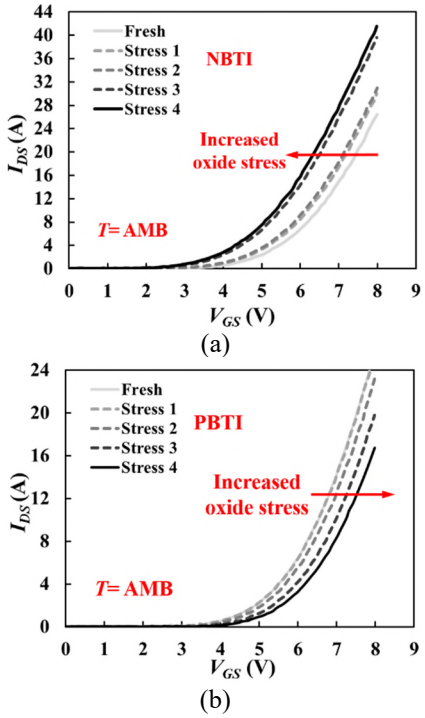


Fig. 1 Gate transfer characteristics measured at ambient temperature. SiC MOSFETs subjected to (a) negative gate bias and (b) positive gate bias, from [45]

Table I. High temperature gate bias stresses for evaluation of BTI [45]

	NBTI	PBTI
Stress 1	-25 V, 150 °C, 30 minutes	25 V, 150 °C, 30 minutes
Stress 2	-25 V, 150 °C, 30 minutes	28 V, 150 °C, 30 minutes
Stress 3	-30 V, 150 °C, 30 minutes	30 V, 150 °C, 30 minutes
Stress 4	-30 V, 150 °C, 30 minutes	32 V, 150 °C, 30 minutes

for a determined V_{GS} and V_{DS}. The results in [40] show that fast measurement methods are able to measure a larger V_{TH} shift and explain the fundamental role of the delay time after measurement, as the V_{TH} rapidly recovers after stress removal. Referring to the measurements in Fig. 1, which are the conventional gate transfer characteristics obtained by sweeping V_{GS} at a fixed V_{DS}, it is clear that the peak shift of V_{TH} will not be observed, as V_{TH} has recovered after the long recovery phase.

The method presented in [11] uses a gate voltage sweep to determine the gate voltage required to obtain a drain current of 10 mA with V_{DS}=50 mV. The threshold voltage is measured after a pre-stress bias and after stress by sweeping the gate voltage away from the stress value (sweep down for a positive stress and sweep up for a negative stress). This is to avoid recovery after stress removal. Factors like the value of the pre-stress bias, the measurement speed and delay between stress and characterization were evaluated in [11]. Among others, the following recommendations were made: application of a consistent pre-stress sequence of a voltage opposed to the stress, measure the post-stress threshold voltage at the same temperature than the stress and re-apply the stress bias for a short period in the case of stress interruption before measurement (delay).

The method proposed in [18, 42] consists in a complex measure-stress-measure sequence which uses pre-conditioning for achieving V_{TH} measurement after stress which is non-dependent on the delay after stress removal. This technique could be highly suitable for qualification tests, where a large batch of devices has to be characterized after stress removal [28]. The preconditioning method [18, 42] is able to eliminate the recoverable shift of V_{TH}, which is not application relevant and highlights the limitations of JEDEC methods like JESD 241 [46] for determining V_{TH} shifts in SiC MOSFETs.

In [1, 47] a method using a measure-stress-measure technique, capable of applying short stress pulses of 100 ns and characterizing the V_{TH} with a delay of 1 µs was used to validate capture emission time maps. This method can characterize the V_{TH} shift resulting from both DC and AC gate stresses, providing information about the fast recovery time components, which is not captured when using precondition-based methods. The impact of the V_{TH} shift on the ON-state resistance was also investigated in [1, 47].

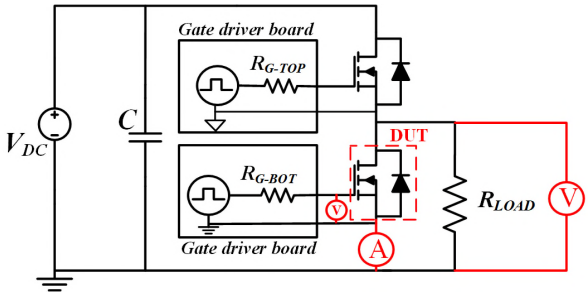
A method that uses the body diode forward voltage as an indicator for V_{TH} shift was presented [45]. Using a sensing current to measure the body diode forward voltage (V_{SD}), V_{TH} shift and recovery was measured indirectly due to the body effect in SiC MOSFETs. This was demonstrated for both positive and negative gate stresses. However, this method will be not applicable if there is an antiparallel Schottky diode since the sensing current will flow through the Schottky diode instead of the MOSFET body diode. The limitations of this method include the temperature dependency of V_{SD} and the requirement of a calibration relationship between V_{SD} and V_{TH}. V_{SD} is temperature dependent and the calibration relationship will only be valid at a defined temperature. Moreover, the method will be sensitive to self-heating of the device [45].

BTI induced V_{TH} shift in SiC MOSFETs has been investigated on the fundamental level [1, 2, 8-19, 28, 40-43], at the application level [1, 8, 48] and also its implications on testing [26, 49]. This paper contributes to this research topic by presenting the use of shoot-through currents resulting from crosstalk in a converter leg as a tool for assessing the impact of BTI-induced threshold voltage shifts in SiC MOSFETs, expanding the analysis and preliminary results presented in [50]. In the next sections the method is developed, and characterization results are presented. It will be shown how the methodology is able to capture the impact of the peak V_{TH} shift and capture the sub-sequent recovery after stress removal.

III. Experimental Set-up and Crosstalk Evaluation in SiC MOSFETs

The experimental test rig for evaluating the impact of crosstalk and shoot-through currents is shown in Fig. 2(a) while the circuit schematic is shown in Fig. 2(b) [50]. It consists of a half-bridge configuration with a resistance R_{LOAD} of 500 Ω connected in parallel with the bottom device. Both devices are driven by gate driver boards based on the gate driver IC HCNW-3120. It is possible to change gate resistances of the devices in converter leg (R_{G_TOP} and R_{G_BOT}). The equipment used for measuring the signals identified in Fig. 2(b) was: a

(a)



(b)

Fig 2 (a) Experimental test rig for crosstalk characterization
(b) Electrical schematic of the test rig

current probe model TCP-312 from Tektronix for measuring the parasitic turn-ON current, a differential voltage probe model TA043 from Pico Electronics for measuring the parasitic gate voltage of the bottom device and a differential voltage probe model GDP-100 from GW Instek for measuring the drain-source voltage of the bottom device. The waveforms were captured using an oscilloscope Wavesurfer 104MXs-B from Lecroy and the driving signals were generated using a waveform generator model TDS2024C.

In the test rig, the high-side device is the driving device that is switched, while the bottom side device is the device under test (DUT) which is evaluated for BTI. Before the top device is switched (when both devices are OFF), the entire DC voltage falls across the top device since R_{LOAD} is much smaller than the OFF-state resistance of the power devices. As the top device is turned ON, the DC voltage is transferred to the bottom device with a drain-source voltage switching rate dV_{DS}/dt [29, 51] that depends on R_{G_TOP} and its parasitic gate-drain capacitance C_{GD_TOP}. The switching rate dV_{DS}/dt can be modelled using (1) [52], where V_{GG} is the gate driver voltage and V_{GP} the Miller Plateau voltage.

$$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{GP}}{R_{G\_TOP} C_{GD\_TOP}} \quad (1)$$

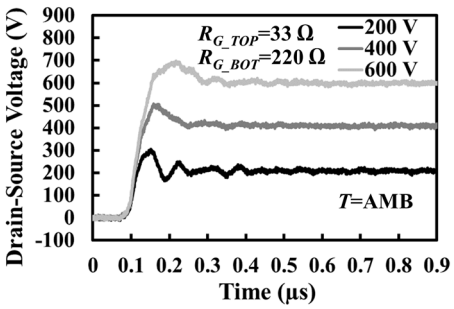
The imposed dV_{DS}/dt couples with the low side device gate-drain parasitic capacitance C_{GD_BOT} to generate a current in the gate loop of the DUT. This Miller capacitance feedback current, given by $C_{GD\_BOT} \cdot dV_{DS}/dt$, charges the low side gate-source capacitance C_{GS_BOT} to a voltage that is determined by the low

side gate resistance R_{G_BOT}. In a basic approximation, the parasitic gate-source voltage V_{GSpara} is given by (2) [29].

$$V_{GSpara} = R_{G-BOT} C_{GD\_BOT} \frac{dV_{DS}}{dt} \left(1 - e^{-\frac{t}{R_{GBOT}(C_{GS\_BOT}+C_{GD\_BOT})}}\right) \quad (2)$$

If the parasitic gate voltage exceeds the threshold voltage, a shoot-through current flows through both devices. Because the MOSFET is driven into saturation (V_{GS} is marginally above V_{TH}), the peak shoot-through current is sensitive to the threshold voltage. Using the test-rig shown in Fig. 2, crosstalk measurements have been performed on a planar SiC MOSFET from Littelfuse at 3 different DC link voltages. The typical threshold voltage at 25 °C for this 1200 V/18 A SiC MOSFET is 2.8 V, according to its datasheet.

Fig. 3(a) to (c) shows the V_{DS} transient across the low side DUT, the parasitic V_{GS} measured on the DUT and resulting shoot-through current flowing through the DUT respectively. A clear semi-short circuit is observable in the measurements, due to the partial turn-ON of the bottom device when its blocking a high voltage. For these measurements, R_{G_TOP} was 33 Ω and R_{G_BOT} was 220 Ω. This combination of R_{G_TOP}/R_{G_BOT} values, although not used in practical converters, was chosen to increase the sensitivity of the shoot-through current to the BTI-induced V_{TH} shift, as it will be demonstrated later. In real-world applications, the choice of the R_{G_TOP}/R_{G_BOT} combination is made to minimize both shoot-through currents [29] and switching losses. It can be seen from Fig. 3 that the parasitic V_{GS} voltages and shoot-through currents increase with DC link voltage and will strongly depend on the threshold voltage and the C_{GS}/C_{GD} ratio of the DUT [51].



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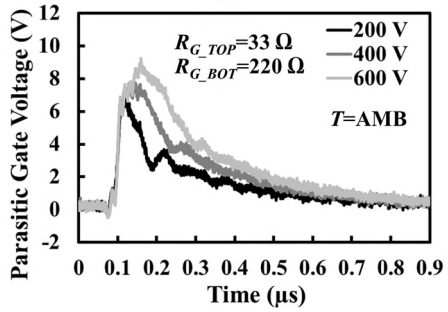

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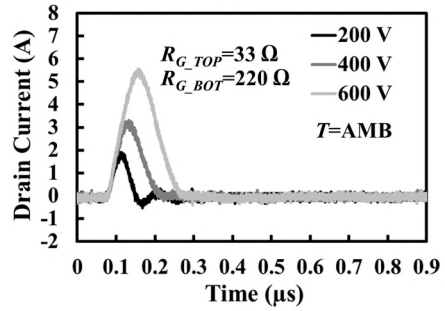


(c)

Fig. 3 Evaluation of crosstalk for a SiC MOSFET planar from Littelfuse at different DC link voltages (a) Drain-source voltage transient of the DUT (b) Parasitic gate voltage of the DUT (c) Shoot-through current of the DUT

The profile of the parasitic gate voltage and shoot-through current depends on the device type, the high side gate resistance (R_{G_TOP}) and the low side gate resistance (R_{G_BOT}). Fig. 4 shows the parasitic V_{GS} measurements for a wide range of SiC MOSFETs from different vendors, including 3 planar SiC MOSFETs and a trench SiC MOSFET. The devices are identified in Table II. The package of these devices is TO-247 and the current ratings are specified for a case temperature of 100 °C.

Table II. SiC MOSFETs. Device identification and characteristics

Device Identification	Voltage Rating	Current Rating	Gate Structure	Manufacturer
Littelfuse Planar	1200 V	18 A	Planar	Littelfuse
Wolfspeed Planar	900 V	15 A	Planar	Cree/Wolfspeed
ST Planar	1200 V	16 A	Planar	ST Microelectronics
ROHM Trench	650 V	15 A	Trench	ROHM

The measurements were performed using the same DC link voltage, R_{G_TOP} and R_{G_BOT}, hence, the differences in parasitic V_{GS} are due to the different parasitic capacitances specific to the device type. It can be seen from Fig. 4 that there are significant differences in the parasitic gate voltage waveforms.

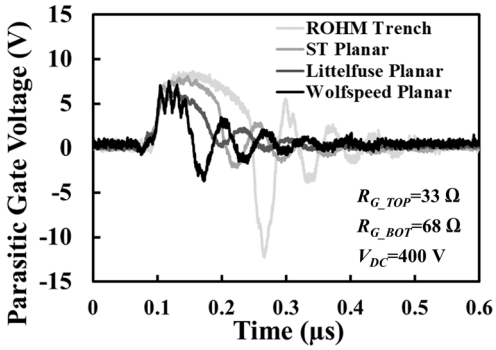
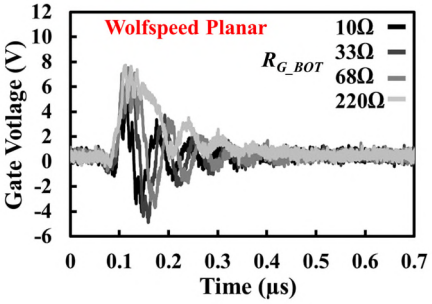


Fig. 4 Parasitic gate voltage for different SiC MOSFETs including planar and trench devices. Ambient temperature

In designing the experiment, careful consideration must be made when choosing the values of R_{G_TOP} and R_{G_BOT}. This is because a shoot-through current that is highly sensitive to V_{TH} is required since it will be used to track the V_{TH}. A small R_{G_TOP} and large R_{G_BOT} causes high parasitic V_{GS} and shoot-through currents. Conversely, a large R_{G_TOP} and small R_{G_BOT} causes a smaller parasitic V_{GS} and shoot-through current. The combination of gate resistances to obtain a good shoot-through



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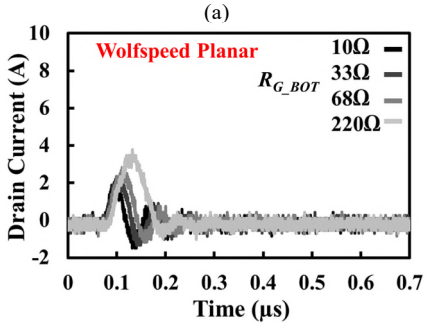
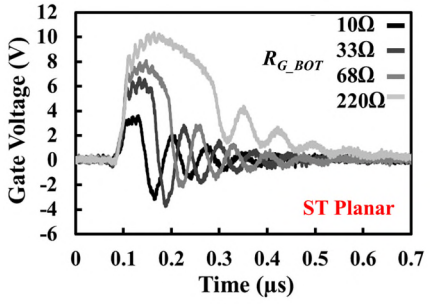


(b)

Fig. 5 Wolfspeed Planar. R_{G_TOP}= 33 Ω. V_{DC}=400 V (a) Induced parasitic gate voltage (b) Drain current



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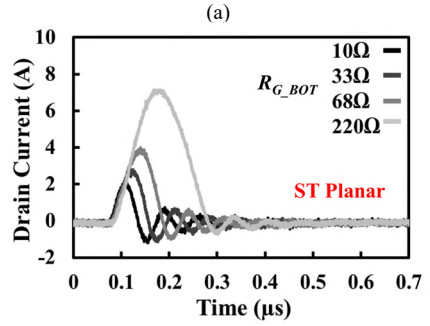
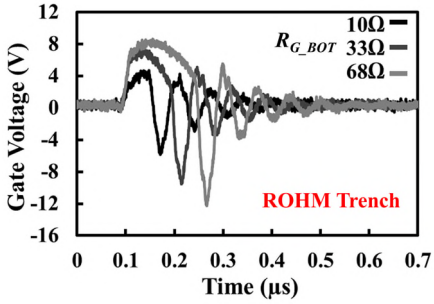


(b)

Fig. 6 ST Planar. R_{G_TOP}= 33 Ω. V_{DC}=400 V (a) Induced parasitic gate voltage (b) Drain current



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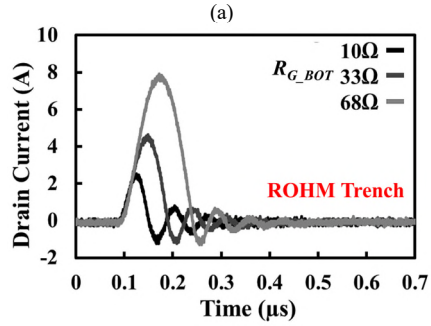


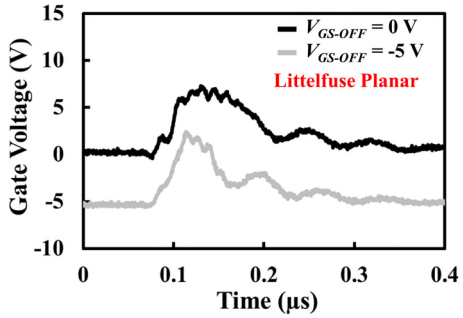
(b)

Fig. 7 ROHM Trench. R_{G_TOP}= 33 Ω. V_{DC}=400 V (a) Induced parasitic gate voltage (b) Drain current

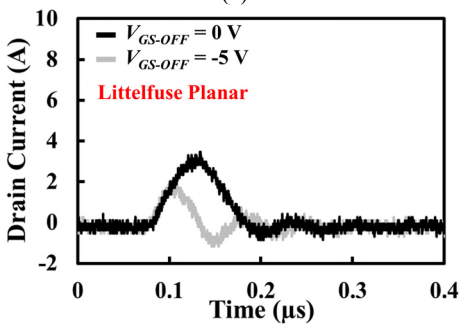
current will depend on the device technology since each device will have different sensitivities to crosstalk. Hence, for the purpose of this experiment, what is desired is for R_{G_TOP} to be smaller than R_{G_BOT}. If the gate resistances are too small (meaning high dV_{DS}/dt), the measurements will be prone to high oscillations due to the combination of fast transients and parasitic inductances.

To show this, measurements have been performed using a wide range of high and low side gate resistances to determine the optimal combination for maximizing the sensitivity of the shoot-through current to V_{TH}. The test circuit in Fig. 2 was used and the DC link voltage was set to 400 V. For all measurements R_{G_TOP} was fixed at 33 Ω and a range of R_{G_BOT} was used to adjust the shoot-through current. Fig. 5 to Fig. 7 show the parasitic gate voltage and shoot-through currents for the Wolfspeed Planar, the ST Planar and the ROHM Trench respectively. Analyzing the results, the different devices exhibit dissimilar parasitic turn-ON characteristics. The Wolfspeed Planar is the least prone to parasitic turn-ON while the ROHM Trench presents the highest shoot-trough current, even with a lower $R_{G\text{-}BOT}$ value.

Another important point to consider is the capacitance charging current through the bottom device, which is unrelated to parasitic turn-ON. This current is the charging current of the $C_{DS\text{-}BOT}$ capacitance and will increase with reduced R_{G_TOP} (due to increasing dV_{DS}/dt). It can be measured by setting the gate turn-OFF voltage $V_{GS\text{-}OFF}$ of the DUT to a negative voltage, thereby ensuring that the device does not parasitically turn ON [29] and measuring only the capacitive charging current. Fig. 8(a) shows the parasitic gate voltages and Fig. 8(b) shows the measured shoot-through currents for the Littelfuse Planar under 2 measurement conditions. In both cases R_{G_TOP}/R_{G_BOT} is 33Ω/100 Ω, but in (i) $V_{GS\text{-}OFF}$=0 V (resulting in a measured peak current around 4 A) and in (ii) $V_{GS\text{-}OFF}$=-5 V (corresponding to measured peak current of around 2 A). As observed in Fig. 8(a), the parasitic gate voltage is below 1 V when $V_{GS\text{-}OFF}$ is -5 V, thereby ensuring that the bottom side device does not parasitically turn-ON. In this situation the measured current



(a)



(b)

Fig. 8 Impact of negative gate voltage for turn-OFF on the shoot-through current. Littelfuse Planar and R_{G_TOP}/R_{G_BOT} = 33Ω/100 Ω (a) Parasitic V_{GS} voltage (b) Shoot-through current

corresponds to the capacitive charging of the low side device (DUT) when subjected to the imposed dV_{DS}/dt.

IV. BTI And Impact On Shoot-Through Current

In section II different methods for characterization of BTI-induced threshold voltage shifts were presented, ranging from the use of the transfer characteristics to novel measure-stress-measure techniques. In this paper, instead of just extracting the V_{TH} shift after stress, the impact of V_{TH} shift on the shoot-through current is evaluated. This approach can show the implications of the V_{TH} shift due to BTI in an operating converter scenario.

A. Accelerated stress tests and long recovery time

First, it is important to demonstrate that a shift of threshold voltage after gate stress will affect the measured shoot-through current. This is done using accelerated gate stress tests. For this initial characterization, the device selected is the Wolfspeed Planar. The device was subjected to accelerated negative gate stresses and the shoot-through current from crosstalk was measured using the test rig presented in Fig. 2, with a DC link voltage V_{DC}=400 V. Similar to the approach used for the measurements shown in Fig. 1, a long recovery was allowed between the end of the stress and the characterization measurements to allow sufficient time for V_{TH} recovery from charge relaxation, thereby characterizing the impact of the permanent V_{TH} shift on the shoot-through current.

The results are shown in Fig. 9. The gate voltages stresses were -25 V for 1 hour at 150 °C, with characterization at ambient temperature after 16 hours recovery with V_{GS}=0, followed by -30 V for 1 hour at 150 °C and characterization at ambient temperature after 16 hours recovery at V_{GS}=0. The accelerated stress values were selected based on the previous work of the authors [45], which resulted in threshold voltage shifts of -330 mV and -890 mV. Since the stress voltage was negative, the resulting downward shift in V_{TH} causes a higher peak shoot-through current and larger shoot-through charge.

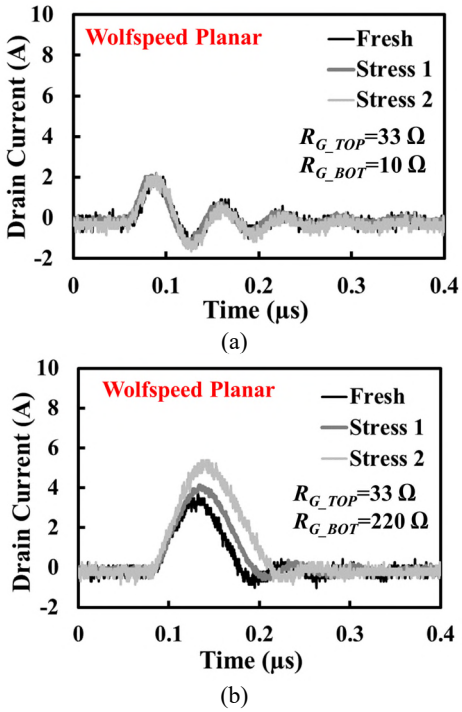


Fig. 9 Measured shoot-through current for unstressed and negative gate bias stressed device. Wolfspeed Planar.
(a) R_{GTOP}/R_{GBOT} = 33Ω/10Ω, (b) R_{GTOP}/R_{GBOT} = 33Ω/220Ω

Fig. 9(a) shows the shoot-through currents transients measured with R_{G_TOP}/R_{G_BOT} of 33 Ω/10 Ω whereas Fig. 9(b) shows shoot-through measurements with a gate resistance combination of 33 Ω/220 Ω. When the gate resistance combination R_{G_TOP}/R_{G_BOT} is 33Ω/10Ω, the measured current in Fig. 9(a) shows no apparent impact of the V_{TH} shift caused by BTI. This is because, as described in section III, this current is just the drain-source capacitance charging current and not the shoot-through current resulting from parasitic turn-ON. However, as shown in Fig. 9(b), using the resistor combination of R_{G_TOP}/R_{G_BOT} = 33 Ω/220 Ω, the impact of the BTI-induced V_{TH} shift on the shoot-through current becomes clear.

Fig. 9 illustrates the impact of permanent V_{TH} shift after stress however, from the point of view of the application, it is important to evaluate the peak shift in the range of microseconds after stress removal and during the transient recovery. The next section will demonstrate how this can be done using the shoot-through current.

B. Short recovery time after stress removal

As was stated in section II, after removal of the stress, the V_{TH} shift caused by BTI recovers within the duration of stress removal and V_{TH} measurement. This may disguise the true extent of BTI and its implications in the application, hence it is important to evaluate the transient shift of V_{TH}. The objective of this investigation is studying how the method can be used to evaluate the impact of BTI-induced shifts on the operation of a converter leg and the impact of the stress and recovery. This can be done using the circuit shown in Fig. 2 and the stress/characterization sequence shown in Fig. 10.

First, the DUT, which is the bottom side device in Fig. 2, is subjected to positive or negative gate stress at a stress voltage V_{STRESS} at a defined temperature T. This is done using a standard unipolar gate driver circuit which can drive the gate of the DUT at 0 V/+ V_{STRESS} for PBTI or a modified unipolar gate driver which can drive the gate at -V_{STRESS}/0V for NBTI. The stress is applied during a time t_{STRESS}, as shown in Fig. 10 for PBTI evaluation.

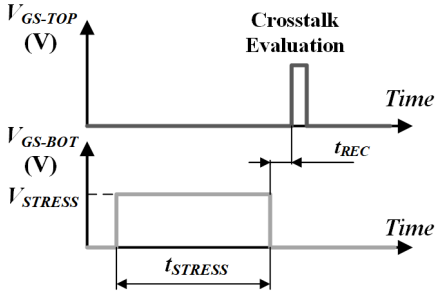


Fig. 10 Stress and Measurement pulses used for characterizing V_{TH} shift and recovery using crosstalk

After the stress voltage is removed, the high side device is triggered with a gate pulse that also parasitically turns ON the bottom side device through crosstalk. The time duration between the end of the stress pulse and the triggering of the high side device is the recovery time t_{REC} as shown in Fig. 10.

As the shoot-through current is affected by the value of the threshold voltage, by varying the recovery time, it is possible to capture the V_{TH} recovery using the shoot-through current. For characterizing the non-stressed DUT, the shoot-through current is measured without applying any stress to the bottom device, holding the gate at 0 V. This technique minimizes the time between stress and characterization and enables the evaluation of the impact of BTI in a more application-oriented test scenario. The proposed technique has been evaluated for positive and negative gate bias stresses for the four devices presented in Table II, measuring the shoot-through current before subjecting the device to the stress and 500 µs after stress removal. The stress voltage was +20 V for 10 s (for PBTI) and a -25 V during 10 s (for NBTI). The DC link was adjusted to 400 V and the measurements were performed at ambient temperature. The two stress values were selected in order to show that the method is applicable for both nominal gate voltage stresses (+20 V) and accelerated gate stresses (-25 V). The selection of the gate resistances was R_{G_TOP}/R_{G_BOT} of 33 Ω/220 Ω for the planar MOSFETs and 33 Ω/68 Ω for the ROHM Trench.

The results for the positive stress in Fig. 11 show how the shoot-through current decreases due to V_{TH} rise from negative charge trapping. The shoot-through charge Q_{ST}, calculated by means of integrating the shoot-through current over time, is summarized in Table III. The results for the negative stress are shown in Fig. 12, with the calculated shoot-through charges presented in Table IV. An increase of the shoot-through current and charge after stress is clearly observable, as a result of the reduction of V_{TH} caused by positive charge trapping.

Table III. Shoot-through charge before and after stress.
Positive Gate Stress. (+20 V/ 10 s, Ambient temperature)

Device	Q_{ST} – *Before stress* (µC)	Q_{ST} – *After stress,* T_{REC}=*500* µs (µC)	Charge ratio (%)
Littelfuse Planar	0.316	0.247	-21.8
Wolfspeed Planar	0.210	0.179	-14.9
ST Planar	0.970	0.566	-41.7
ROHM Trench	0.772	0.591	-23.4

Table IV. Shoot-through charge before and after stress
Negative Gate Stress. (-25 V/ 10 s, Ambient temperature)

Device	Q_{ST} – *Before stress* (µC)	Q_{ST} – *After stress,* T_{REC}=*500* µs (µC)	Charge ratio (%)
Littelfuse Planar	0.425	0.534	+25.5
Wolfspeed Planar	0.271	0.333	+22.9
ST Planar	1.218	1.709	+40.4
ROHM Trench	1.322	1.977	+49.5

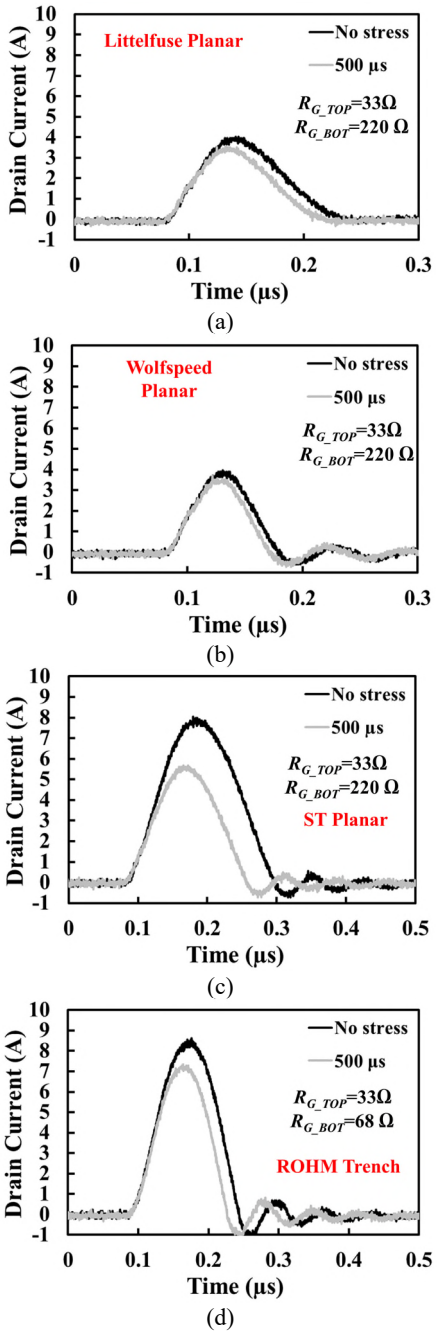


Fig. 11 Shoot-through current before and after positive gate stress (+20 V/ 10 s., Ambient temperature, Recovery time = 500 µs)
(a) Littelfuse Planar (b) Wolfspeed Planar
(c) ST Planar (d) ROHM Trench

Analyzing the results for the positive stress, the device that is most affected by the positive gate stress is the ST Planar, with a reduction of the shoot-through charge of around -40% measured 500 µs after stress removal. The Wolfspeed Planar is the least affected by the positive V_{GS} stress, while the impact of the gate stress is similar for the Littelfuse Planar and ROHM Trench.

Evaluating the negative gate stress results, the ROHM Trench is the most affected by the gate stress (increase of shoot-through charge of 49.5%), followed by the ST Planar, with the

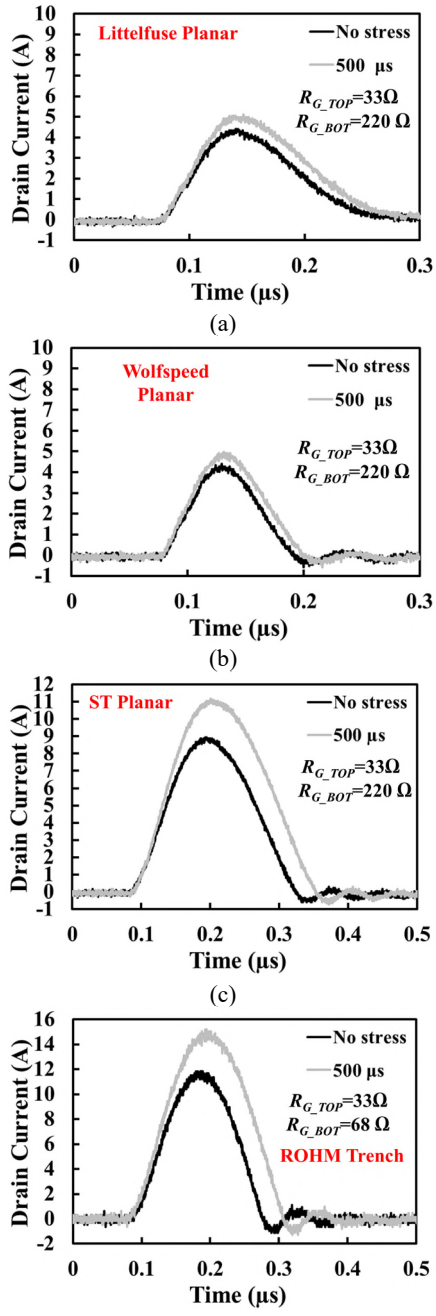


Fig. 12 Shoot-through current before and after negative gate stress (-25 V/ 10 s., Ambient temperature, Recovery time = 500 µs) (a) Littelfuse Planar (b) Wolfspeed Planar (c) ST Planar (d) ROHM Trench

Littelfuse Planar and Wolfspeed Planar being affected similarly. An important observation is that despite -25 V being an accelerated stress test, the planar devices present a similar sensitivity to the evaluated positive and negative stresses, whereas the evaluated ROHM Trench is clearly more sensitive to the negative stress.

A variation in the measured shoot-through current and charge due to the change of the gate driver for applying the negative gate stresses has been identified. The authors attribute this to the different parasitic elements of the gate driver circuit required for switching from -V_{STRESS} to 0 V. The role of the parasitic elements of the gate driver circuit was investigated in [53], where its impact on the parasitic gate voltage was demonstrated. In [53], using experimental measurements it is shown that the ratio between the parasitic gate inductance and the parasitic source inductance affects the peak parasitic gate voltage. The resonance between the parasitic gate inductance and the input capacitance can also increase the gate voltage oscillations [54]. Recommendations for minimizing the parasitic inductances for achieving the best performance regarding parasitic turn-ON are also given in [54]. The implication of this is that initial reference measurement before stress has to be done with the gate driver circuit that will be used for the specific gate stress.

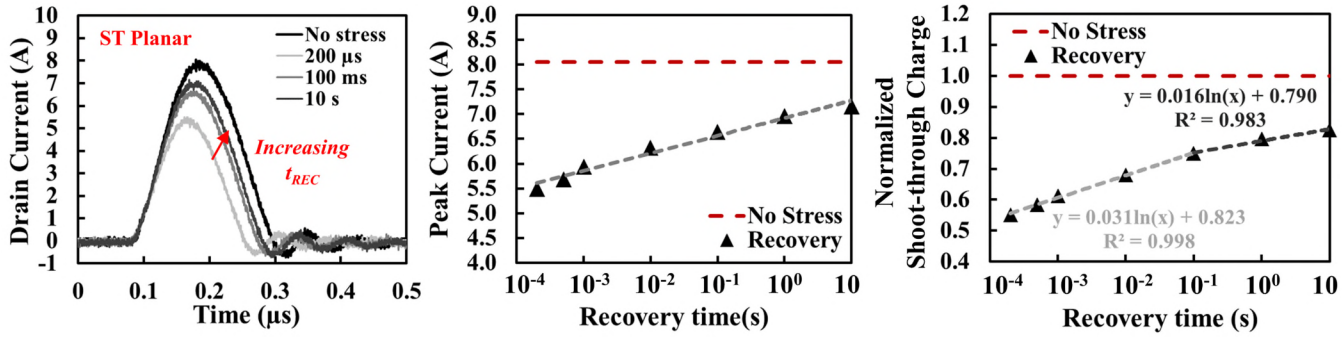
V. Characterization Results

This section will demonstrate how the proposed methodology can be used for characterizing the impact of the recovery time and temperature for both positive and negative gate stresses. The study will be performed using the devices which are more sensitive to crosstalk currents, namely the ST Planar and the ROHM Trench. It is worth to mention that the lower susceptibility to parasitic turn-ON of the Littelfuse Planar and Wolfspeed Planar will make the characterization using this method more challenging. The DC link voltage used for this test is 400 V and the gate resistor combinations are R_{G_TOP}/R_{G_BOT} of 33 Ω/220 Ω for the ST Planar and 33 Ω/68 Ω for the ROHM Trench. It is important to highlight that the objective of these investigations is not comparing the gate reliability of the devices, but showing how the method can capture the differences between them.

A. Impact of recovery time

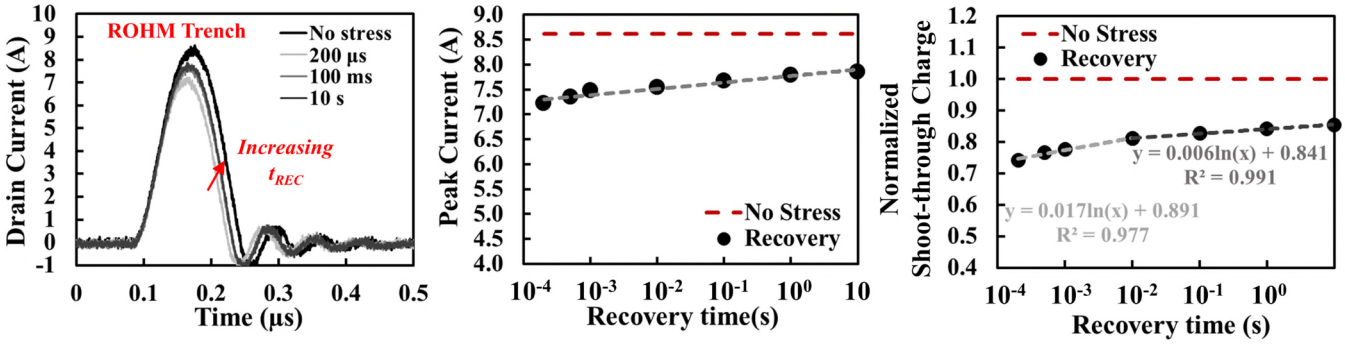
The previous section presented the importance of measuring the impact of the V_{GS} stress shortly after stress removal to quantify the peak V_{TH} shift before transient recovery [8, 18, 19]. By varying the time interval between stress removal and shoot-through measurement (t_{REC} in Fig. 10), it is possible to quantify the impact of the recovery time on the measurements. The ST Planar and the ROHM Trench were subjected to both positive (V_{STRESS}=20 V during 10 s at ambient temperature) and negative gate stresses (V_{STRESS}=-25 V during 10 s at ambient temperature), characterizing the shoot-through current energy as a function of the recovery time after stress removal.

It should be noted that for characterizing the recovery of V_{TH}, every measurement was performed using a new stress pulse and allowing a recovery time of 180 s between measurements. This is because multiple measurements of V_{TH} at different recovery times after defined stress pulse will mean that the device is subjected to repetitive shoot-through currents within a short duration, especially for characterization during the initial stages of the recovery phase. This will inevitably cause the self-heating of the device, thereby causing a V_{TH} shift due to the temperature increase (therefore disguising V_{TH} shift due to BTI). An aluminum block was attached to the case of the



(a) (b) (c)

Fig. 13 ST Planar. Positive gate stress and recovery using crosstalk. V_{STRESS}= 20 V, t_{STRESS}=10 s, Ambient temperature, (a) Measured shoot-through current transient, (b) Peak Current as function of recovery time, (c) Normalized shoot-through charge as function of recovery time



(a) (b) (c)

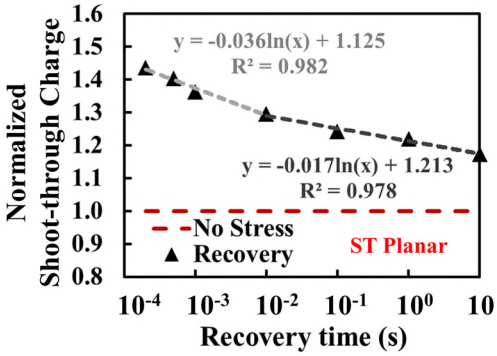
Fig. 14 ROHM Trench. Positive gate stress and recovery using crosstalk. V_{STRESS}= 20 V, t_{STRESS}=10 s, Ambient temperature, (a)Measured shoot-through current transient, (b) Peak Current as function of recovery time, (c) Normalized Shoot-through charge as function of recovery time

discrete TO-247 device thereby acting as a heatsink and enabling the observation of the temperature increase during the measurements. During the performed tests, the measured temperature increase was lower than 1 °C, hence the impact of temperature on the measured shoot-through currents can be considered negligible.

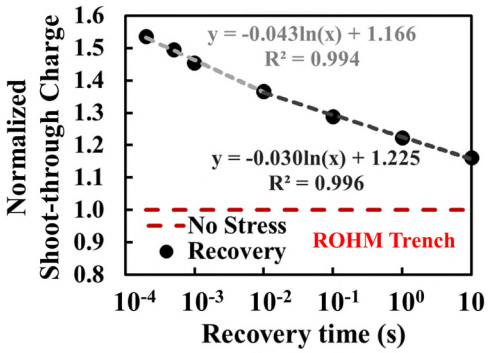
Starting with the positive stress, the results for the ST Planar are shown in Fig. 13. Fig. 13(a) shows the measured shoot-through current transient for different t_{REC} values (ranging from 200 µs to 10 s) and the non-stressed state. Fig. 13(b) shows the measured peak shoot-through current and tracks its value against the non-stressed peak current while Fig. 13(c) plots the normalized shoot-through charge for the different recovery times. The shoot-through charge is a more accurate variable as it can compensate the lack of resolution and noise of the peak current measurement. Fig. 14 shows the results for the positive bias stress of the ROHM Trench.

Analyzing the results, it is evident how the shoot-through current reduces after the positive stress and gradually increases as the recovery time is increased. This correlates to the trapped charges being released and V_{TH} reducing back to the pre-stress value. Comparing both devices, the same stress causes a higher reduction of the shoot-through current in the ST Planar. The rate of change of the peak current suggests a logarithmic dependence of the recovery, which is clearly observed by analyzing the shoot-through charge, normalized respect to the pre-stress value in Fig. 13(c) and Fig. 14(c). For both SiC MOSFETs different slopes are observed during the recovery phase. This change in slope can be explained as the release of different amounts of traps with short and long characteristic time constants. From the results in Fig. 13 and Fig. 14, fast traps play a key role in the threshold voltage shift (range of µs to ms). The capture and release of traps with different time constants is discussed in [28] and it is one of the main reasons why fast methods for BTI characterization in SiC MOSFETs are required. After 10 s, from the results in Fig. 13(c) and Fig. 14(c), the shoot-trough charge recovers to 82.5% of its value in the ST Planar and 85.4% in the ROHM Trench. Both SiC MOSFETs recover to similar post-stress values after 10 s, but the peak charge is higher for the ST Planar, indicating a faster post-stress recovery.

The results for the negative gate stress are shown in Fig. 15, which presents the normalized shoot-through charge as function of the recovery time for the ST Planar and the ROHM Trench. Similar to the positive stress results, a change of slope during the recovery is observed for both SiC MOSFETs. The presence of traps with small characteristic time constants (fast emission times) is more apparent for the ST Planar, with a faster recovery during the first 10 ms after stress removal. Considering the recovery after 10 s, in the case of the ST Planar the shoot-trough charge recovers to a value 17.4% higher than its pre-stress value, whereas for the ROHM Trench the recovery is to a 16.2% higher. As the peak charge variation is higher in the ROHM Trench, this indicates a faster recovery for this device.

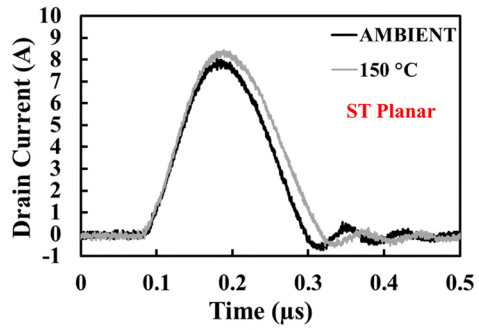


(a)

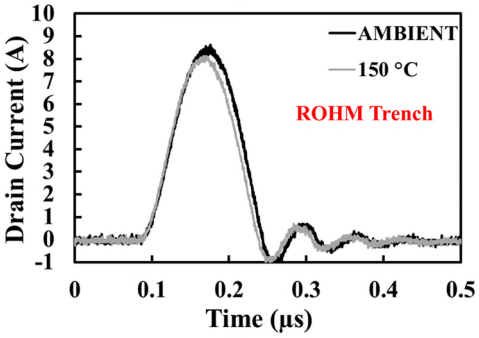


(b)

Fig. 15 Normalized Shoot-through charge as function of recovery time for a negative gate stress (V_{STRESS}= -25 V, t_{STRESS}=10 s, Ambient temperature) (a) ST Planar (b) ROHM Trench



(a)



(b)

Fig. 16 Impact of temperature on shoot-through current. (a) ST Planar (b) ROHM Trench

B. Impact of temperature

In order to evaluate the impact of temperature on the recovery of threshold voltage, the previous measurements were repeated for the same devices at a case temperature of 150 °C. This temperature was set using a small heater attached to the discrete device and allowing enough time for the junction and case temperatures to reach steady state. Before evaluating the impact of BTI on the shoot-through current, it is important to evaluate the impact of temperature on the shoot-trough current of the devices under study. This is shown in Fig. 16 for both the ST Planar and the ROHM Trench. It can be observed that in the case of the ST Planar, the shoot-through current increases with temperature, where in the case of the ROHM Trench the shoot-through current reduces with temperature hence presenting opposite temperature sensitivities. However, the scope of this investigation is not the evaluation of the temperature dependency of the shoot-trough current but the impact of BTI stresses on crosstalk and its temperature dependency. To that end, stress and recovery characterization measurements were performed at high temperature using the devices characterized in section V.A. The results for the positive gate bias stress at 150 °C are shown in Fig. 17 for the ST Planar and Fig. 18 for the ROHM Trench. Both SiC MOSFETs were also subjected to negative gate bias stresses at 150 °C (V_{STRESS}=-25 V during 10 s) and the results are shown in Fig. 19, which shows the normalized shoot-through charge as function of the recovery time. The calculated shoot-through charges before and after stress, for a recovery time of 500 µs, are shown in Table V and Table VI for the positive stress and the negative stress respectively.

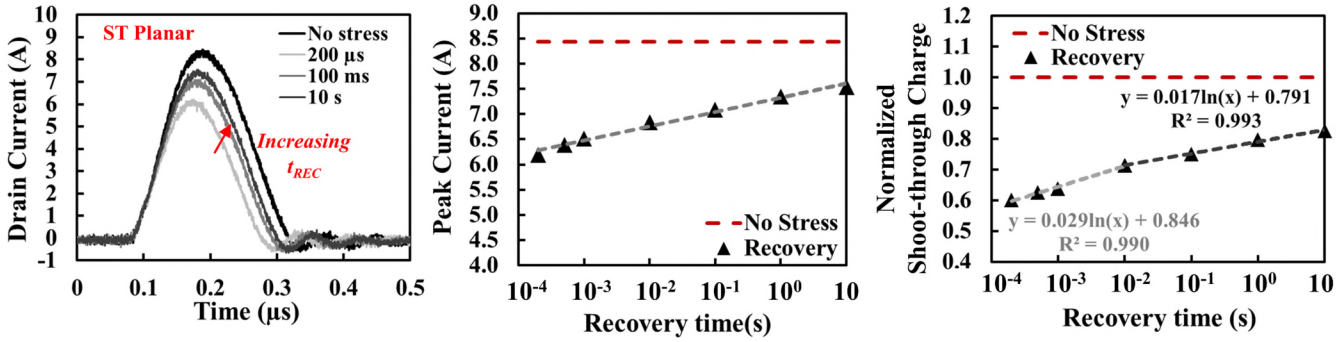
Table V. Shoot-through charge before and after stress
Positive Gate Stress. (+20 V/ 10 s, 150 °C)

Device	Q_{ST} – *Before stress* (µC)	Q_{ST} – *After stress,* t_{REC}=*500* µs (µC)	Charge variation (%)
ST Planar	1.114	0.698	-37.4
ROHM Trench	0.711	0.490	-31.0

Table VI. Shoot-through charge before and after stress
Negative Gate Stress. (-25 V/ 10 s, 150 °C)

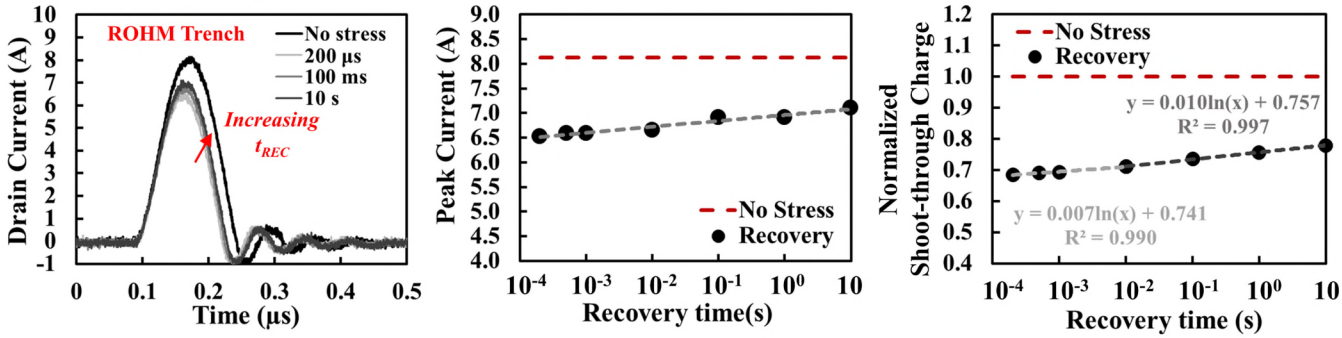
Device	Q_{ST} – *Before stress* (µC)	Q_{ST} – *After stress,* t_{REC}=*500* µs (µC)	Charge variation (%)
ST Planar	1.327	1.779	+34.0
ROHM Trench	1.040	1.608	+54.6

Comparing the shoot-through charge variation for the positive stress, the results show that the ROHM Trench is more affected than the ST Planar, increasing the reduction of the shoot-through charge from -23.4 % at ambient to -31% at 150 °C. In the case of the ST Planar, there is a reduction of the shoot-through charge of -37.4% at 150 °C, compared with -41.7% at ambient. These values were measured for a recovery time of 500 µs hence fast charges may have not been detected.



(a) (b) (c)

Fig. 17 ST Planar. Positive gate stress and recovery using crosstalk. V_{STRESS}= 20 V, t_{STRESS}=10 s, T=150 °C, (a) Measured shoot-through current transient, (b) Peak Current as function of recovery time, (c) Normalized shoot-through charge as function of recovery time



(a) (b) (c)

Fig. 18 ROHM Trench. Positive gate stress and recovery using crosstalk. V_{STRESS}= 20 V, t_{STRESS}=10 s, T=150 °C, (a)Measured shoot-through current transient, (b) Peak Current as function of recovery time, (c) Normalized Shoot-through charge as function of recovery time

Considering the negative gate stresses at 150 °C, in the case of the ROHM Trench the shoot-through charge increases more at high temperatures, 54.6% at 150 °C compared with 49.5% at ambient temperature. As was the case of the positive stresses at high temperature, the ST Planar is less affected, with an increase of the shoot-through charge of 34% at 150 °C, compared with an increase of 40.4% at ambient temperature.

Analyzing the recovery transients at 150 °C for the positive stress, a slower recovery is observed in the case of the ROHM Trench. This slow recovery is already noticeable on the shoot-trough current transients in Fig. 18(a) and observing the normalized shoot-through charge in Fig. 18(c), the impact of temperature on the recovery transient becomes clearer. For this device, the invariability of the measured shoot-through current for short recovery times indicates that at high temperature there are more trapped charges with large emission times. In the case of the ST Planar, at 150 °C the fast traps become more dominant below 10 ms whereas at ambient the change of slope was at 100 ms.

Comparing the recovery transients after negative gate stress in Fig. 15 and Fig. 19, the ROHM Trench shows a similar post-stress recovery at 150 °C and at ambient, whereas the ST Planar recovers faster at 150 °C, with the inflection point at 100 ms.

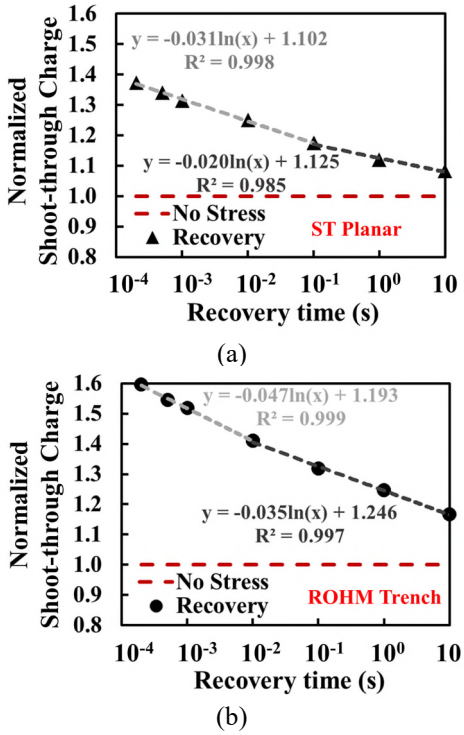


Fig. 19 Normalized Shoot-through charge as function of recovery time for a negative gate stress (V_{STRESS}= +20 V, t_{STRESS}=10 s, 150 °C) (a) ST Planar (b) ROHM Trench

VI. Conclusions

BTI remains a challenge in SiC power MOSFETs. Traditional methods of capturing V_{TH} shift by measuring the

static characteristics usually do not characterize the transient nature of the problem i.e. the time dependency of V_{TH} due charge de-trapping. This paper has demonstrated a method for characterizing V_{TH} shift using shoot-through currents/charge induced from crosstalk between the two power devices in a half-bridge. Since the shoot-through current/charge is highly sensitive to V_{TH}, it can be used as a technique for characterizing BTI in SiC MOSFETs as well as its impact on a converter leg. Positive gate bias stress causes the V_{TH} to increase and the shoot-through current to reduce while negative gate bias stress causes the V_{TH} to reduce and the shoot-through current to increase. By measuring the shoot-through current/charge at different times after gate voltage stress removal, the time and temperature dependency of the V_{TH} recovery can be analyzed. The technique has been applied to SiC MOSFETs from different manufacturers by evaluating the impact of BTI for both positive and negative gate voltage stresses at ambient temperature and 150 °C. The technique has demonstrated that it is possible to capture the implications of V_{TH} shift and recovery within several hundreds of microseconds after gate voltage stress removal thereby giving further insight into the nature of charge trapping/de-trapping and the different time constants associated with the traps.

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